ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention	FIFO Memory Devices Having Multi-Port Cache Memory Arrays Therein that Support Hidden EDC Latency and Bus Matching and Methods of Operating Same

Application Number: 10/612849
Confirmation Number: 6889
First Named Applicant: Mario Au
Attorney Docket Number: 5646-42DVIP
Art Unit: 2186
Search string: (6557053 or 6366529 or 6259648 or 5442747 or 4888741).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
GJP	1	6557053	2003-04-29	Bass et al.	B1	710	29
↑	2	6366529	2002-04-02	Williams et al.	B1	365	239
|	3	6259648	2001-07-10	Kragick	B1	365	230.05
↓	4	5442747	1995-08-15	Chan et al.		395	164
GJP	5	4888741	1989-12-19	Malinowski		365	230.05

Signature

Examiner Name	Date
GARY J. PORTKA	11/28/05